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Jiajia Chen; Chip-Hong Chang; Vinod, A.P.;

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### A 2.7-/spl mu/W/MHz transmission-gate-based 16-bit multiplier for digital hearing aids

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# A Continuous-Time ADC/DSP/DAC System With No Clock and With Activity-Dependent Power Dissipation

Schell, B.; Tsividis, Y.;

Solid-State Circuits, IEEE Journal of

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### Input-specific Dynamic Power Optimization for VLSI Circuits

Fei Hu; Agrawal, V.D.;

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### Low power datapath design using transformation similar to temporal localization of SFGs

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Keliu Shu; Sanchez-Sinencio, E.; Silva-Martinez, J.; Embabi, S.H.K.;

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Abstract A 2.1-GHz monolithic frequency synthesizer with robust phase switching prescaler and loop capacitance scaling Shu, K.; Sanchez-Sinencio, E.; Silva-Martinez, J.; Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on Volume: 4 Digital Object Identifier: 10.1109/ISCAS.2002.1010576 Publication Year: 2002, Page(s): IV-791 - IV-794 vol.4 **IEEE Conferences** AbstractPlus | Full Text: PDF (293 KB) (C) Cuick > Abstract Enhanced dual-transition probabilistic power estimation with selective supergate analysis Fei Hu; Agrawal, V.D.; Computer Design: VLSI in Computers and Processors, 2005. ICCD 2005. Proceedings. 2005 IEEE International Conference on Digital Object Identifier: 10.1109/ICCD.2005.49 Publication Year: 2005, Page(s): 366 - 369 **IEEE Conferences** AbstractPlus | Full Text: PDF (184 KB) Quek ) Abstract

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Juan-Chico, J.; Ruiz de Clavijo, P.; Bellido, M.J.; Acosta, A.J.; Valenia, M.;

Circuits and Systems, 2000. Proceedings, ISCAS 2000 Geneva. The 2000 IEEE International Symposium on

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### Stability analysis of APC systems

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Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '81.

Volume: 6

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### Transition analysis on FPGA for multiplier-block based FIR filter structures

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# Enhanced dual-transition probabilistic power estimation with selective supergate analysis

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